Tcon Application Note

TV MS Development Team

2015. 07. 03

LG Display

Tcon Application Note update List

< History Table >

No.	Version	Event	Change point	Remark
1	V0.0		First Draft	

Series	Inch	Version	Date	Etc
V16 UHD 60Hz M+	43	V0.1	2015. 07. 03	DRD

Items	Setting

< Voltage setting >

Voltage	Measurement Value
	Voltage
VDD	16.0 V
HVDD	8 V
VCC18 (VEPI)	1.8 V
VGH (25℃)	30.0 V
VGH (0℃)	32.0 V
VGL1	-5.0 V
VGL2	-15 V

Voltage was measured on Source PCB.

< P-gamma >

	Gamma Ref.	Value	Unit
Positive Voltage	Gamma1	15.0	VDC
	Gamma4	-	
	Gamma5	11.99	
	Gamma6	11.02	
	Gamma9	8.42	
Negative Voltage	Gamma10	7.54	
	Gamma13	5.12	
	Gamma14	4.23	
	Gamma15	-	
	Gamma18	1.11	
VCOM		4.21	

Items	Setting

< Power Integration IC Option >

Register	Name	Address	Bit							
			7	6	5	4	3	2	1	0
Vcom Operation	Discharing [7]	14h	0	0	0	0	0	1	0	0
	Temp Comp [6:3]									
	Vcom 1 Gain [2:0]									

Register	Name	Address	Bit							
			7	6	5	4	3	2	1	0
Vcom & L/S Option	Vcom2 Gain [7:5]	17h	1	0	1	1	0	1	0	0
	Temp Comp [4:3]									
	L/S & TSD [2][1][0]									

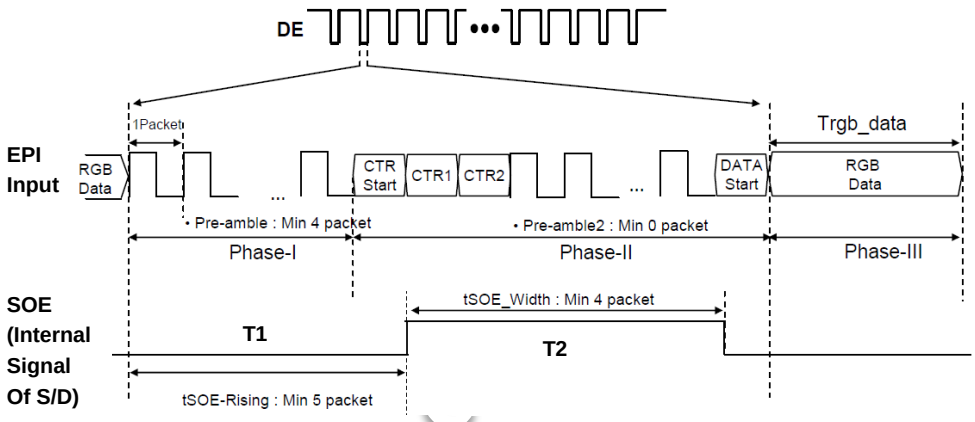
Items	Setting

< Input Condition >

Item	Value	Unit
H Total	4400	Tclk
V Total	2250	LINE
CLK Freq.	74.25	MHz

※Below timing was made by this input condition.

< Source D-IC Control >

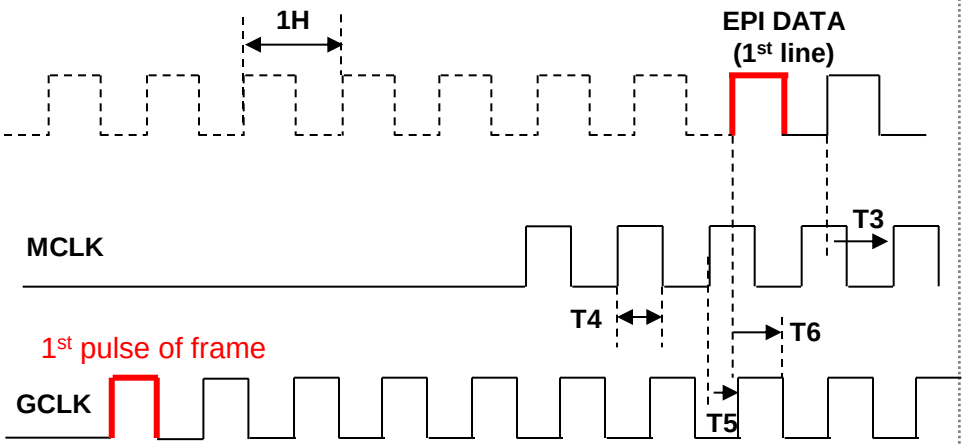


SOE rising / falling edge

T1	Refer to 8Page
T2	Refer to 8Page

※ SOE can't be measured. Just set SOE timing in EPI signal correctly and check it.

< GIP : MCLK/GCLK Control – Frame start condition >



MCLK rising / falling edge

T3	166 clocks 2235 ns
T4	10 clocks 134.68 ns

GCLK rising / falling edge

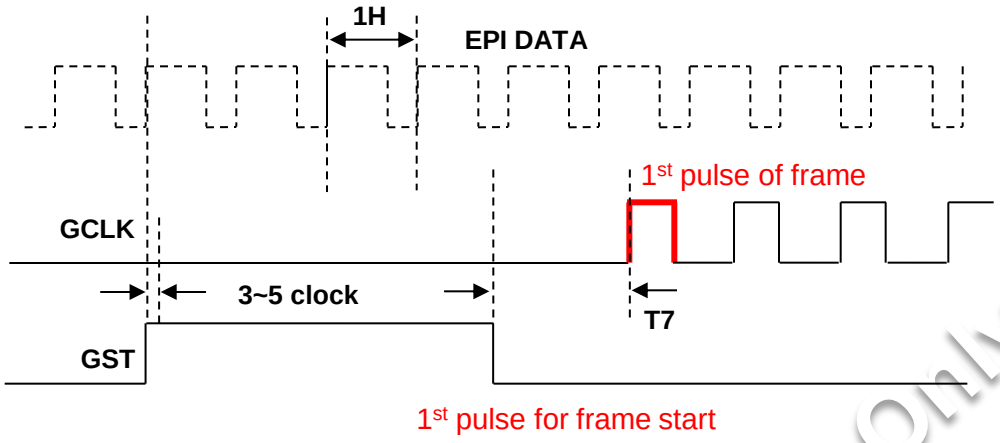
T5	80.8 clocks 1087 ns
T6	114.9 clocks 1546 ns

※ 1st MCLK : between 5th and 6th GCLK pulse

※ 1st line EPI data : around 9th period of GCLK

Items	Setting

< GIP : GST control – Frame start condition >



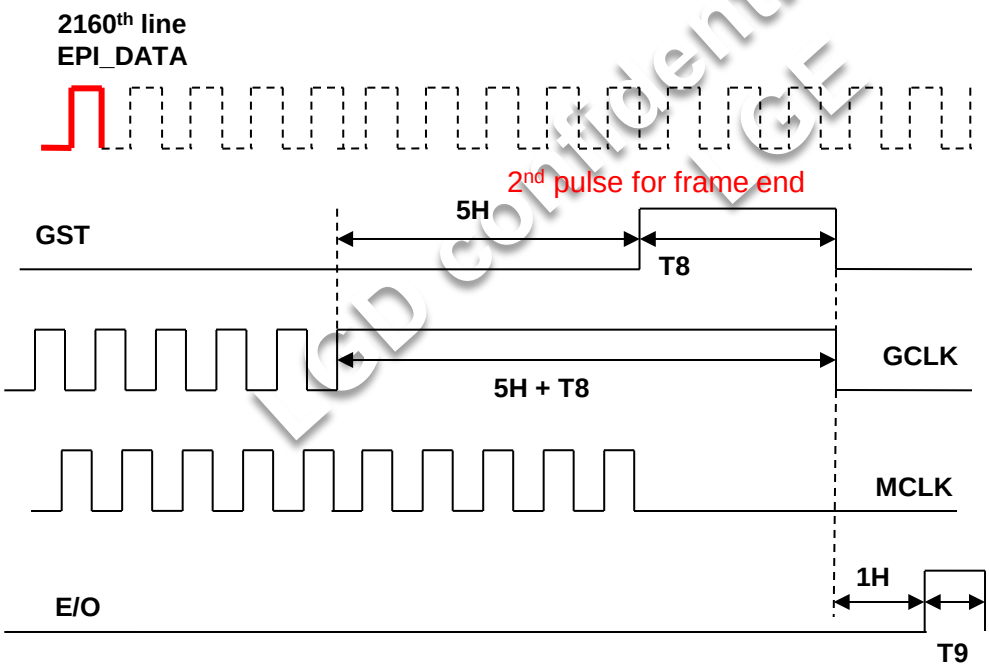
GST falling edge at frame start

T7	40 Clock 558.25 ns

※ High width of GST is around 2H.

※ GST may have 2 pulse. One is for frame start, the other is for frame end

< GIP : MCLK/GCLK control – Frame end condition >



GST width at frame end

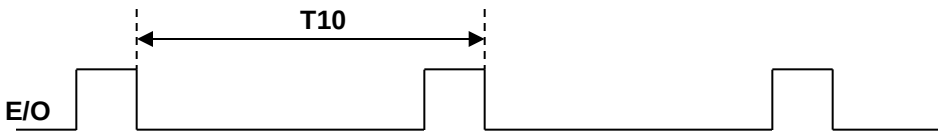
T8	3 H

E/O width at frame end

T9	48 clocks 646.46 ns

※ Maximum of T9 : 1H

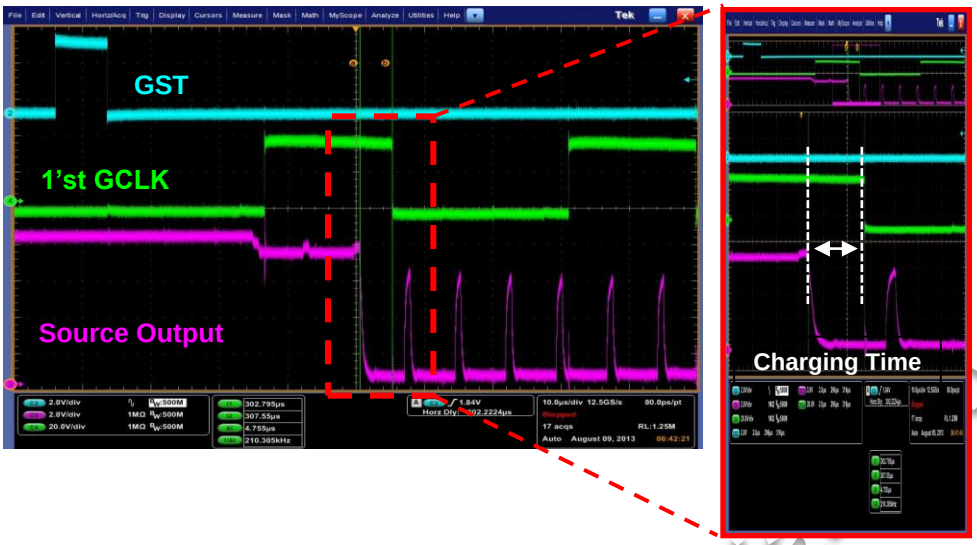
< GIP : E/O period >



E/O period

T10	63 Frames

※ T10 : 2 ~ 5 sec

Items	Setting
< Charging Time Test Method > 	Charging Time: 2.1 us ※ 1'st GCLK is - CLK1 at normal mode. - CLK8 at reverse mode. ※ Source output can be measured with LTD_OUT or Z-OUT on FFC connector. ※ When user measure source output, use full white(255gray) pattern & Charge-Share Mode.

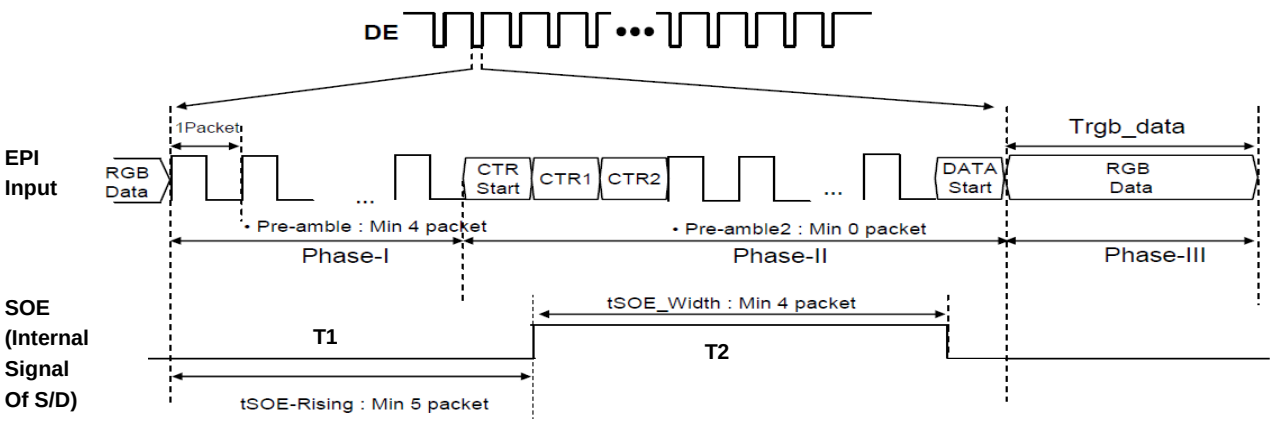
1. Control Option Mapping

	Name	BIT	Description	Setting Value	Remark
CTR2	Dummy	C[1:0]		**H**	“H” fix
	POL	C2	Polarity signal	**H/L**	Changes every horizontal line depends on inversion type
	MODE	C3	Output reset function Mode	**L**	
	H2DOT	C4	Horizontal 2-Dot inversion	**H**	
	LTD1	C5	LTD Mode Selection 1	**H**	
	LTD2	C6	LTD Mode Selection 2	**H**	
	PWRC1	C7	Power Control Mode 1	**H**	
	PWRC2	C8	Power Control Mode 2	**L**	
	PWRC3	C9	Power Control Mode 3	**L**	
	Reserved	C10		**L**	
	GSP	C11	Gate start pulse bit	**H/L**	
	CSC	C12	Charge Share Control	**L**	
	Reserved	C13		**L**	“L” fix
	Reserved	C14		**L**	“L” fix
	LbR	C15	Shift direction control	**H**	
	H_4ChC	C16	Horizontal 4-CH inversion bit	**L**	
	EQ1	C17	Equalizer mode control pins	**L**	
	EQ2	C18	Equalizer mode control pins	**L**	
	H2DOT_2D	C19	Horizontal 2D inversion bit	**L**	
	TEST	C[23:20]	Test mode	**L**	
	Reserved	C[25:24]		**L**	“L” fix
	Dummy	C[27:26]		**L**	“L” fix

※ LSB is transmitted at first, always.

1-1. Source D-IC Control Setting

Control Data	EPI.	T1 (Packet)	T2 (Packet)
SOE	EPI1	0	24
	EPI2	0	24
	EPI3	0	25
	EPI4	0	25
	EPI5	0	26
	EPI6	0	26
	EPI7	0	26
	EPI8	0	26
	EPI9	0	25
	EPI10	0	25
	EPI11	0	24
	EPI12	0	24



ex) Output (Source D-IC #3)

- T1 : 0 packet + 5 packet → 5 packet
- T2 : 26packet + 4 packet → 30 packet

1-2. Source D-IC Control Setting

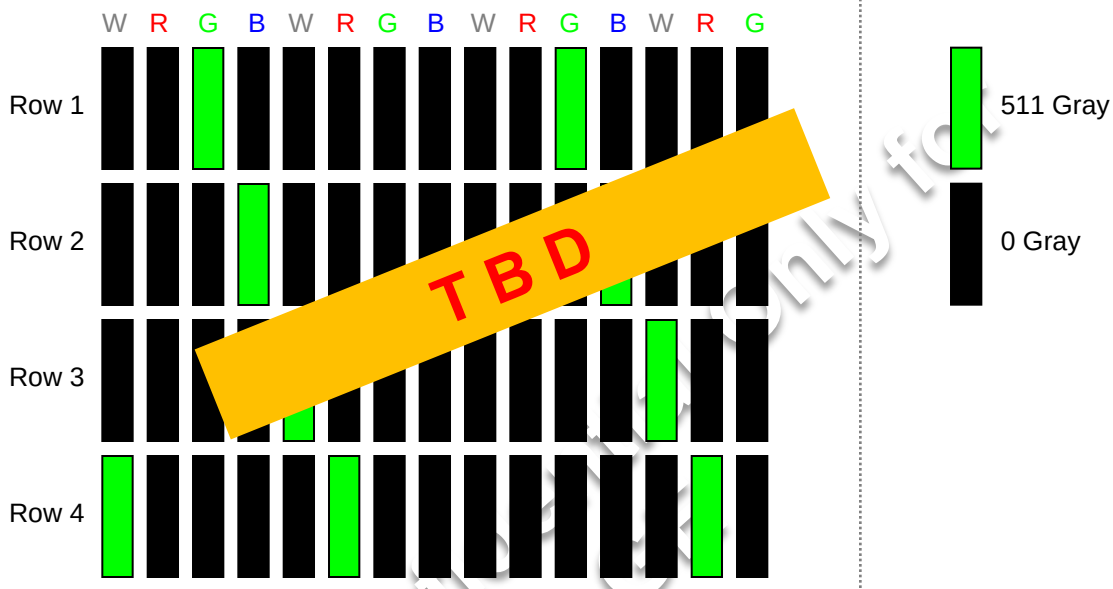
Repeat every horizontal line depends on Case 1~8

	INV4	INV3	INV2	INV1	INV_EN
1	1	0	1	0	1
2	0	0	0	0	1
3	0	0	0	0	1
4	0	1	0	1	1
5	0	1	0	1	1
6	1	1	1	1	1
7	1	1	1	1	1
8	1	0	1	0	1

Items	Setting

< VCOM Adjustment >

Flicker Pattern



ITEM	Condition
Inversion Method	Vertical 4 Dot Inversion

Items	Setting

< Gate power sequence >

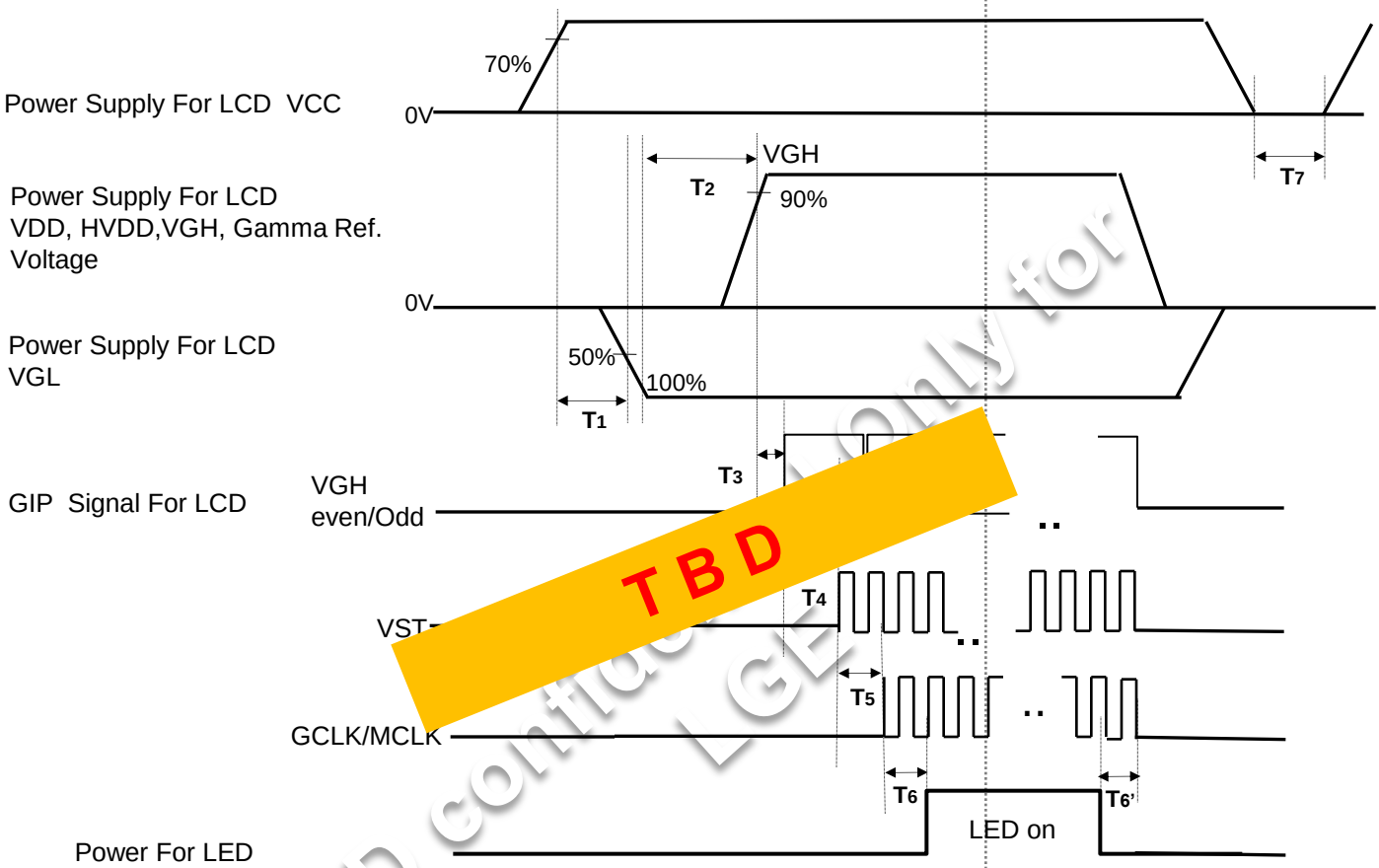


Table 7. POWER SEQUENCE

Ta= 25±2°C, fv=60Hz, Dclk=74.25MHz

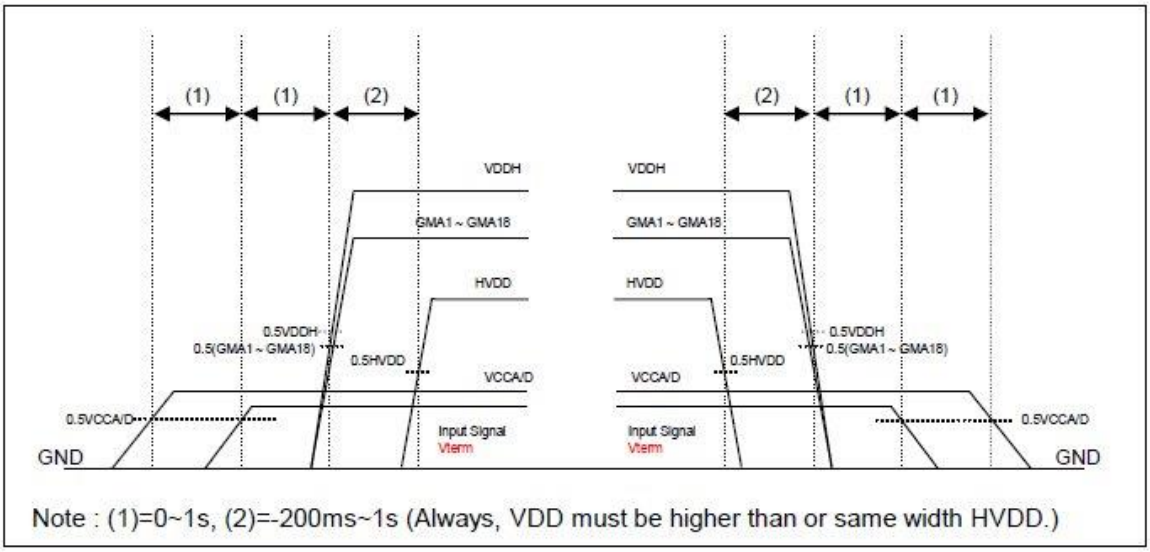
Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	0.5		-	ms	
T2	0.5		-	ms	
T3	0		-	ms	
T4	10		-	ms	2
T5	0		-	ms	
T6 / T6'	20		-	ms	
T7	2		-	sec	

Note : 1. Power sequence for Source D-IC must follow the Case1 & 2.
※ Please refer to Appendix V for more details.
2. VGH Odd signal should be started “High” status and VGH even & odd can not be “High at the same time.
3. Power Off Sequence order is reverse of Power On Condition including Source D-IC.
4. VDD_odd/even transition time should be within V_ blank

Items	Setting

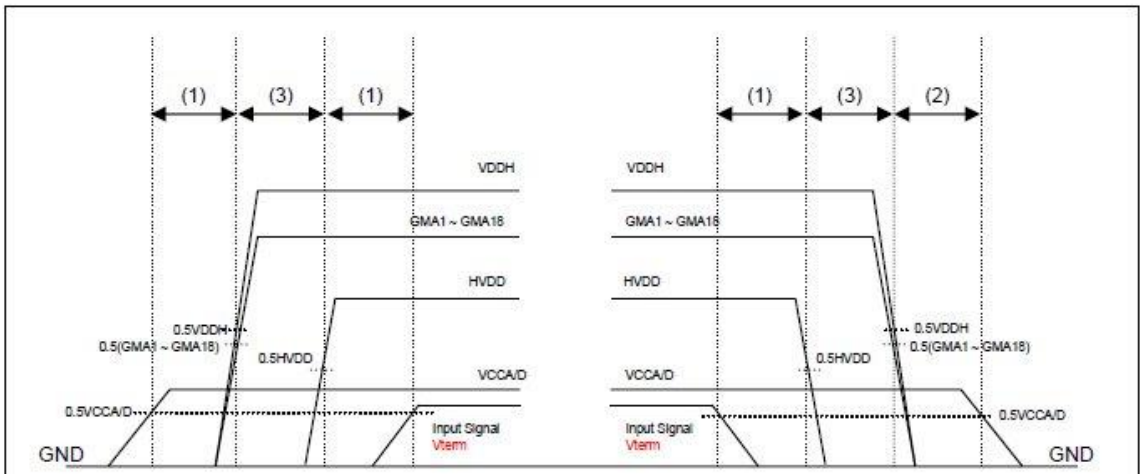
< Source power sequence >

1. CASE1



Note : (1)=0~1s, (2)=-200ms~1s (Always, VDD must be higher than or same width HVDD.)

2. CASE2



Note : (1)=0~1s, (2)=-200ms~1s,
(3)=-200ms~1s (Always, VDD must be higher than or same width HVDD.)

※ When VCC and VDD power sequence reversed, high voltage control signal (level shifter output signal) not unknown status,

Input Signal : EPI